

**AMENDMENTS TO THE CLAIMS:**

The follow listing of claims replaced all prior versions and listings of claims in the application.

**Listing of Claims:**

1-14. (canceled)

15. (currently amended) A method for fabricating a circuit component, comprising:  
providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer on said second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening;

providing an exposed metallization structure over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump configured ~~[[used ]]~~for a package interconnect, wherein said metal bump has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump; and

after said providing said exposed metallization structure and prior to wafer testing of said semiconductor wafer, performing a sputter etching process with an argon gas.

16-26. (canceled)

27. (currently amended) A method for fabricating a circuit component, comprising:  
providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer over said semiconductor wafer and on said second region, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening;

providing an exposed metallization structure over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump ~~[[used ]]~~configured for a package interconnect, wherein said metal bump has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump; and

after said providing said exposed metallization structure and prior to wafer testing of said semiconductor wafer, performing an ion milling process with an argon gas.

28-34. (canceled)

35. (currently amended) The method of claim 15, after said performing said sputter etching process, further comprising ~~contacting said metal bump with having~~ a testing probe contact said metal bump.

36. (currently amended) The method of claim 27, after said performing said ion milling process, further comprising ~~contacting said metal bump with having~~ a testing probe contact said metal bump.

37. (currently amended) A method for fabricating a circuit component, comprising:  
providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer on said second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening;

providing an exposed metallization structure directly on said passivation layer, on said first region and over said semiconductor wafer, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump configured ~~[[used ]]~~for a package interconnect, wherein said metal bump has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump; and

after said providing said exposed metallization structure and prior to wafer testing of said semiconductor wafer, performing an ion milling process with an inert gas.

38. (previously presented) The method of claim 37, wherein said inert gas comprises an argon gas.

39. (currently amended) The method of claim 37, wherein said inert gas comprises [[an ]]a helium gas.

40. (canceled)

41. (currently amended) The method of claim 37, after said performing said ion milling process, further comprising ~~contacting said metal bump with having~~ a testing probe contact said metal bump.